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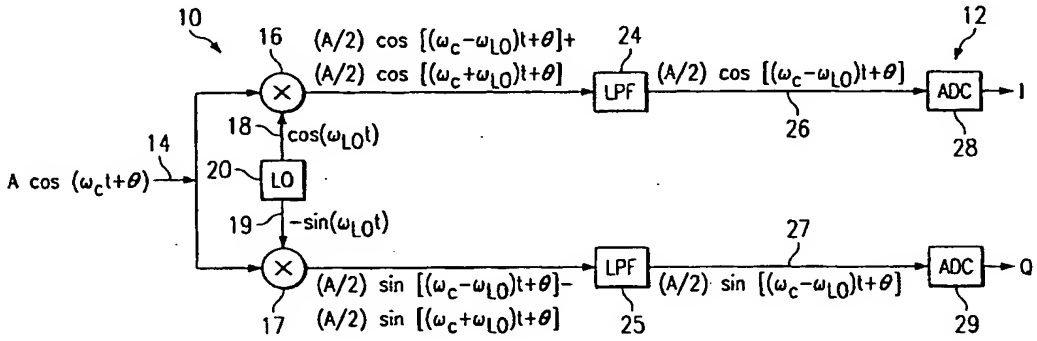

(57) Abstract: An apparatus for quadrature tuner error correction includes an offset correction circuit adapted to receive a digital in-phase signal and a digital quadrature signal from a quadrature tuner. The offset correction circuit has an in-phase circuit comprising a summer adapted to receive the digital in-phase signal, subtract an in-phase offset estimate therefrom, and generate an offset corrected in-phase signal, and a feedback loop adapted to integrate the offset corrected in-phase signal, multiply the integrated offset corrected in-phase signal by a first adjustable constant, and generate the in-phase offset estimate. The offset correction circuit has a quadrature circuit comprising a summer adapted to receive the digital quadrature signal, subtract a quadrature offset estimate therefrom, and generate an offset corrected quadrature signal, and a feedback loop adapted to integrate the offset corrected quadrature signal, multiply the integrated offset corrected quadrature signal by a second adjustable constant, and generate the quadrature offset estimate.

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APPARATUS AND METHOD FOR QUADRATURE TUNER ERROR CORRECTION

TECHNICAL FIELD OF THE INVENTION

This invention is related in general to the field of electrical and electronic circuits. More particularly, the invention is related to apparatus and a method for quadrature tuner error correction.

BACKGROUND OF THE INVENTION

A block diagram of an ideal quadrature tuner 10 and digitizer 12 is shown in FIGURE 1. An unmodulated input carrier signal 14 is represented by $A\cos(\omega_C t+\theta)$. Unmodulated input carrier signal 14 has a peak amplitude A, radian frequency ω_C, and an arbitrary phase of θ radians. Input carrier signal 14 is mixed by mixers 16 and 17 with two signals 18 and 19 generated by a local oscillator (LO) 20. Signals 18 and 19 are represented by $\cos(\omega_{LO}t)$ and $-\sin(\omega_{LO}t)$, which both have a normalized amplitude of 1, radian frequency ω_{LO}, and normalized phase of 0 radians. The resulting signals are:

$$A\cos(\omega_c t+\theta)\cos(\omega_{LO}t) = (A/2)\cos[(\omega_c-\omega_{LO})t+\theta] + (A/2)\cos[(\omega_c+\omega_{LO})t+\theta]$$

and (1)

$$-A\cos(\omega_c t+\theta)\sin(\omega_{LO}t) = (A/2)\sin[(\omega_c-\omega_{LO})t+\theta] - (A/2)\sin[(\omega_c+\omega_{LO})t+\theta]$$

Ideal lowpass filters (LPFs) 24 and 25 receive these resultant signals and remove only the high frequency components, resulting in analog in-phase (I) and quadrature (Q) signals 26 and 27:

$$I = (A/2)\cos[(\omega_c - \omega_{LO})t + \theta] \quad \text{and} \quad Q = (A/2)\sin[(\omega_c - \omega_{LO})t + \theta] \qquad (2)$$

Analog in-phase and quadrature signals 26 and 27 are converted to digital form by analog-to-digital converters (ADC) 28 and 29 for further processing.

On the other hand, a real quadrature tuner produces offset, gain, and phase errors which reduce the accuracy of the resulting in-phase and quadrature signals. The worst case gain and phase errors of several commercially available tuner devices are in the ±0.5 dB and ±5.0° range, respectively.

Conventional attempts to correct these errors may use analog trimming, adjustments, or calibration. These methods are undesirable due to high cost. Another conventional method uses analog-to-digital converters with wide bandwidths and high speed to digitize the in-phase and quadrature output signals. The requirement of high performance analog-to-digital converters adds substantially to cost and the complexity of the circuit.

SUMMARY OF THE INVENTION

Accordingly, there is a need for a circuit and method that efficiently correct quadrature tuner offset, gain, and phase errors. In accordance with the present invention, apparatus and a method of quadrature tuner error correction are provided which eliminate or

substantially reduce the disadvantages associated with prior circuits or algorithms.

In one aspect of the invention, apparatus for quadrature tuner error correction includes an offset correction portion adapted to receive a digital in-phase signal and a digital quadrature signal from a quadrature tuner. The offset correction portion has an in-phase portion comprising a summer adapted to receive the digital in-phase signal, subtract an in-phase offset estimate therefrom, and generate an offset corrected in-phase signal, and a feedback loop adapted to integrate the offset corrected in-phase signal, multiply the integrated offset corrected in-phase signal by a first adjustable constant, and generate the in-phase offset estimate. The offset correction portion has a quadrature portion comprising a summer adapted to receive the digital quadrature signal, subtract a quadrature offset estimate therefrom, and generate an offset corrected quadrature signal, and a feedback loop adapted to integrate the offset corrected quadrature signal, multiply the integrated offset corrected quadrature signal by a second adjustable constant, and generate the quadrature offset estimate.

In another aspect of the invention, a method of correcting errors in a quadrature tuner includes an offset correction process which receives a digital in-phase signal and a digital quadrature signal from the quadrature tuner. The offset correction process has an in-phase portion which includes the steps of receiving the digital in-phase signal, subtracting an in-phase offset estimate therefrom, and generating an offset corrected in-phase signal, and feeding back the offset

corrected in-phase signal through a first feedback loop, the feedback loop integrating the offset corrected in-phase signal, multiplying the integrated offset corrected in-phase signal by a first adjustable constant, and generating the in-phase offset estimate. The offset correction process also has a quadrature portion with the steps of receiving the digital quadrature signal, subtracting a quadrature offset estimate therefrom, and generating an offset corrected quadrature signal, and feeding back the offset corrected quadrature signal through a feedback loop, the feedback loop integrating the offset corrected quadrature signal, multiplying the integrated offset corrected quadrature signal by a second adjustable constant, and generating the quadrature offset estimate.

In yet another aspect of the invention, apparatus for quadrature tuner error correction includes an offset correction portion adapted to receive a digital in-phase signal and a digital quadrature signal from a quadrature tuner and generating offset corrected in-phase and quadrature signals, a gain correction portion coupled to the offset correction portion adapted to receive the offset corrected in-phase and quadrature signals and generating offset and gain corrected in-phase and quadrature signals, and a phase correction portion coupled to the gain correction portion adapted to receive the gain corrected in-phase and quadrature signals and generating offset, gain and phase corrected in-phase and quadrature signals.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference may be made to the accompanying drawings, in which:

FIGURE 1 is a functional block diagram of an ideal quadrature tuner and digitizer;

FIGURE 2 is a functional block diagram of an embodiment of an offset correction circuit and algorithm constructed according to an embodiment of the present invention;

FIGURE 3 is a functional block diagram of an embodiment of a gain correction circuit and algorithm constructed according to an embodiment of the present invention;

FIGURE 4 is a functional block diagram of an embodiment of a gain control multiplier constructed according to an embodiment of the present invention; and

FIGURE 5 is a functional block diagram of an embodiment of a phase correction circuit and algorithm constructed according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The in-phase and quadrature offset errors produced by a real quadrature tuner may be represented by adding O_I and O_Q, to the respective output signals. The offset errors are DC signals typically in the range of ± 10 millivolts. The offsets are not necessarily matched, and may vary as a function of operating temperature.

The gain error may be represented by multiplying the respective in-phase and quadrature signals by constants G_I and G_Q. Gain mismatch can be expressed in dB using the equation:

$$\text{Gain mismatch (db)} = 20 \log 10 (G_I / G_Q) \quad (3)$$

Gain mismatch is typically in the range of ±1 dB, and may vary as a function of operating temperature.

A phase error of ϕ radians can be represented by adding half of its value to the phase of the in-phase output signal, and subtracting half of its value from the phase of the quadrature output signal.

Therefore, the equations which represent the in-phase and quadrature outputs with offset, gain and phase error sources are:

$$I = O_I + G_I(A/2)\cos[(\omega_c - \omega_{LO})t + \theta + \phi/2] \quad (4)$$
$$Q = O_Q + G_Q(A/2)\sin[(\omega_c - \omega_{LO})t + \theta - \phi/2]$$

Combining the gain and amplitude terms and normalizing results in:

$$I = O_I + A_I \cos[(\omega_c - \omega_{LO})t + \theta + \phi/2] \quad (5)$$
$$Q = O_Q + A_Q \sin[(\omega_c - \omega_{LO})t + \theta - \phi/2]$$

Input of these uncorrected signals with offset, gain and phase errors into a standard demodulator results in substantially degraded performance.

Offset Correction

A functional block diagram of an embodiment of the digital offset correction circuit and algorithm 40 according to the present invention is shown in FIGURE 2. The in-phase and quadrature signals may both be corrected for offset error with the circuit or algorithm shown in FIGURE 2. A summer 42 receives the in-phase or quadrature signal from analog-to-digital converter 28 or 29 (FIGURE 1) as input signal 41 and subtracts an offset estimate 44 from it. Offset estimate 44 is supplied by a multiplier 46, which in effect multiplies an input 48 thereto by a constant 2^{-N}. Multiplier 46 is coupled to an integrator 50, which receives its input from the output of summer 42.

In operation, a near zero offset estimate 44 is first subtracted from the in-phase or quadrature signal input 42, and the resultant output 52 is integrated and fed back through multiplier 46 to form the offset estimate 44. Multiplier 46 may be implemented by a shifter which shifts its input signal right N bits. This circuit and algorithm in essence implement a high pass filter with a cut-off frequency that can be made arbitrarily low by increasing N (and consequently the width of the integrator).

Offset correction circuit and algorithm of the present invention is adapted to function properly with no input signal or noise-only input. However, the circuit or algorithm may not function properly if an unmodulated carrier signal is applied to mixers 16 and 17 with frequency closely matching the frequency of local oscillator 20 (i.e. $\omega_C \approx \omega_{LO}$). This condition can be

avoided by slightly off-tuning local oscillator 20 from the expected range of input frequencies.

In an embodiment of the present invention, an offset correction value controller 45 such as a symmetric limiter as known in the art may be incorporated at the output of multiplier 46 to limit the range of offset correction values if needed.

In an embodiment of the present invention, offset correction value controller 45 may include a correction register, multiplexer, processor and other components (not shown) to allow processor control of the value of offset correction 44 during certain operating conditions, such as temperature variation. The offset correction value may be computed or determined in response to a control input such as a temperature measurement.

Gain Correction

A functional block diagram of an embodiment of a gain correction circuit and algorithm 60 according to the present invention is shown in FIGURE 3. Preferably, gain correction follows offset correction and uses, as input, the in-phase and quadrature output from offset correction circuit and algorithm 40 shown in FIGURE 2. The offset corrected in-phase and quadrature signals 61 and 62 are provided to multipliers 63 and 64, respectively, to be multiplied by initial correction values (near 1). The resulting gain corrected output signals are each squared by a squaring network including squarers 66 and 67, and a difference between the squared values is determined by a summer 68. The difference result is then fed to an integrator 70 and multiplier 72 (shown implemented as a shifter). The output from

multiplier 72 is provided as a gain correction signal to mixer 64 to be mixed with quadrature signal 62. The output from multiplier 72 is also supplied to mixer 63 to be mixed with in-phase signal 61 after it is inverted, as in $()^{-1}$, by an inverter 74.

A feedback loop enable circuit 65 may be needed to disable the feedback loop when no signal or noise inputs are present. For example, feedback loop enable circuit may include a lowpass filter to detect the absence of signal or noise input or to compare the squarer output with a reference signal at the output of squarer 66. Only when the detected power output of the squarer exceeds the predetermined reference value, is the feedback loop enabled.

Preferably, gain correction follows offset correction, since an uncorrected offset value in the in-phase or quadrature signals may erroneously contribute to the squaring power measurement calculations. It may be desirable to disable the gain correction feedback loop until the offset correction loops have settled and stabilized.

An embodiment of the gain offset algorithm may include a gain correction value controller 73 such as a symmetric limiter coupled to the output of shifter 72 to limit the range of gain correction values. Gain correction value controller 73 may also include processor controlled calibration to account for control input such as operating temperature date.

The embodiment of gain correction multipliers 63 and 64 may take advantage of the limited range of the gain control values. Assume that the maximum allowable corrected error is ±0.1 dB. Correction of an overall

(I/Q) gain imbalance of ±1 dB with a maximum error of ±0.1 dB requires I and Q multipliers 63 and 64 each having a maximum gain range of ±0.5 dB and setting error of ±0.05 dB. Given a logarithmic gain control signal and multiplier, settings of -0.45 dB in 0.1 dB steps (10 total) meet the requirement. A maximum gain of +0.5 dB corresponds to a maximum linear correction value of 1.059254, and minimum gain of -0.5 dB corresponds to a minimum linear correction value of 0.944061.

The maximum input control value corresponds to a right shift of $-\log_2(0.059) = 4.08$, or just over 4 bits. The maximum value of K is then just under 1/16. Assuming 3 magnitude bits and 1 sign bit (16 total steps) are adequate for representing the control value, the possible gain selections are shown in Table A below:

Control Bits	Control Value	Gain=1+(val/128)	Gain (db)	Δ Gain, Prev. Value
0111	+7	1.054688	0.4625	N/A
0110	+6	1.046875	0.3979	0.0646
0101	+5	1.039063	0.3328	0.0651
0100	+4	1.031250	0.2673	0.0655
0011	+3	1.023438	0.2012	0.0661
0010	+2	1.015625	0.1347	0.0665
0001	+1	1.007813	0.0676	0.0671
0000	0	1.000000	0.0000	0.0676
1111	-1	0.992188	-0.0681	0.0681
1110	-2	0.984375	-0.1368	0.0687
1101	-3	0.976563	-0.2060	0.0692
1100	-4	0.968750	-0.2758	0.0698
1011	-5	0.960938	-0.3461	0.0703
1010	-6	0.953125	-0.4170	0.0709
1001	-7	0.945313	-0.4885	0.0715
1000	-8	0.937500	-0.5606	0.0721

TABLE A

The results show that the maximum gain setting of 0.4625 dB is less than the specified maximum of 0.5 dB. However, it is 0.5 - 0.4625 = 0.0375 dB from that level, which is within the $\pm$0.05 dB error tolerance. The minimum gain setting of -0.5606 dB is just under the specified minimum of -0.5 dB. The worst case gain step due to resolution limits is 0.0721 dB. The worst case setting error due to resolution limitations is then

$\pm$0.721/2 = $\pm$0.036 dB, which is within the specified limit of $\pm$0.5 dB.

A functional block diagram of an embodiment of a circuit forr efficiently implementing this linear range is shown in FIGURE 4. Multiplier 80 is used to implement multipliers 63 and 64 in FIGURE 3 and includes a multiplier 82 receiving a gain, K, and the in-phase or quadrature signal from offset correction circuitry. The output from multiplier 82 is supplied to a summer 84, which sums the in-phase or quadrature input and the output from multiplier 82.

Multiplier 80 may have a 4-bit two's complement control value input. The output of multiplier 80 is shifted right 7 bits (1/128) from the LSB (least significant bit) of the input in-phase or quadrature signal. Further multiplier logic reductions can be realized through truncation and/or rounding prior to the output, since the 6 or 7 multiplier output LSB's are normally not utilized by output summer 84.

The use of the multiplier 80 also allows the multiplicative inversion, $()^{-1}$, of gain correction circuit shown in FIGURE 3 to be replaced by an additive inversion (two's complement) function, which generally has less complexity.

Phase Correction

A complete phase correction loop requires phase error detection and phase error correction functions. Phase error detection is accomplished by multiplying the in-phase and quadrature signals. Following offset and gain correction, the equations for the in-phase and quadrature signals are:

$$I = A\cos[(\omega_c - \omega_{LO})t + \theta + \phi/2] \qquad (6)$$
$$Q = A\sin[(\omega_c - \omega_{LO})t + \theta - \phi/2]$$

Multiplying the two signals together results in:

$$I \cdot Q = A\cos[(\omega_c - \omega_{LO})t + \theta + \phi/2] \cdot A\sin[(\omega_c - \omega_{LO})t + \theta - \phi/2] \qquad (7)$$
$$I \cdot Q = (A^2/2)\sin[2\cdot(\omega_c - \omega_{LO})t + 2\cdot\theta] - (A^2/2)\sin(\phi)$$

The first term has no DC component, and can be removed by a lowpass filter (or integrator), resulting in the phase error signal:

$$Filtered\ I \cdot Q = -(A^2/2)\sin(\phi) \qquad (8)$$

The remaining unknown value is the amplitude of the input signal. The filtered output of the in-phase or quadrature squarer used to determine signal and/or noise presence for the gain correction algorithm is approximately $A^2/2$ when there is a sufficiently high input signal to noise ratio (SNR). Dividing the filtered I·Q signal by the filtered in-phase or quadrature squarer output results in a phase error detection signal that is approximately equal to $-\sin(\phi)$. Greater accuracy may be

achieved by using a power estimate value generated by a coherent demodulator utilizing the corrected signals.

For every corresponding pair of in-phase and quadrature samples, the cosine and sine terms differ only in the $\phi/2$ term. The identical terms are represented by Θ to simplify the phase error correction equations. The equations for the offset and gain corrected in-phase and quadrature values are:

$$I = A\cos(\Theta + \phi/2) \qquad (9)$$
$$Q = A\sin(\Theta - \phi/2)$$

Given the trigonometric identities:

$$\cos(\alpha+\beta) = \cos(\alpha)\cos(\beta) - \sin(\alpha)\sin(\beta) \qquad (10)$$
$$\sin(\alpha-\beta) = \sin(\alpha)\cos(\beta) - \cos(\alpha)\sin(\beta)$$

Substituting Equations (10) into Equations (9) results in Equations (11):

$$I = A\cos(\Theta)\cos(\phi/2) - A\sin(\Theta)\sin(\phi/2) \qquad (11)$$
$$Q = A\sin(\Theta)\cos(\phi/2) - A\cos(\Theta)\sin(\phi/2)$$

Solving Equations (11) for $A\cos\Theta$ and $A\sin\Theta$ results in:

$$A\cos(\Theta) = [I + A\sin(\Theta)\sin(\phi/2)] / \cos(\phi/2) \qquad (12)$$
$$A\sin(\Theta) = [Q + A\cos(\Theta)\sin(\phi/2)] / \cos(\phi/2)$$

Substituting Equations (12) into Equations (11) results in:

$$I = A\cos(\Theta)\cos(\phi/2) - [Q + A\cos(\Theta)\sin(\phi/2)]\sin(\phi/2)/\cos(\phi/2) \qquad (13)$$
$$Q = A\sin(\Theta)\cos(\phi/2) - [I + A\sin(\Theta)\sin(\phi/2)]\sin(\phi/2)/\cos(\phi/2)$$

Expanding Equations (13) and using the relationship tan $(\phi/2) = \sin(\phi/2)/\cos(\phi/2)$ results in:

$$I = A\cos(\Theta)\cos(\phi/2) - Q\tan(\phi/2) - A\cos(\Theta)\sin(\phi/2)\tan(\phi/2) \qquad (14)$$
$$Q = A\sin(\Theta)\cos(\phi/2) - I\tan(\phi/2) - A\sin(\Theta)\sin(\phi/2)\tan(\phi/2)$$

Rearranging Equations (14) results in:

$$A\cos(\Theta)\cos(\phi/2) - A\cos(\Theta)\sin(\phi/2)\tan(\phi/2) = I + Q\tan(\phi/2) \qquad (15)$$
$$A\sin(\Theta)\cos(\phi/2) - A\sin(\Theta)\sin(\phi/2)\tan(\phi/2) = Q + I\tan(\phi/2)$$

Isolating A cos Θ and A sin Θ in Equations (15) results in:

$$A\cos(\Theta) = [I + Q\tan(\phi/2)]/[\cos(\phi/2) - \sin(\phi/2)\tan(\phi/2)] \qquad (16)$$
$$A\sin(\Theta) = [Q + I\tan(\phi/2)]/[\cos(\phi/2) - \sin(\phi/2)\tan(\phi/2)]$$

The left hand sides of Equations (17) are defined as the corrected in-phase and quadrature values I and Q:

$$I = A\cos(\Theta) = [I + Q\tan(\phi/2)]/[\cos(\phi/2) - \sin(\phi/2)\tan(\phi/2)] \qquad (17)$$
$$Q = A\sin(\Theta) = [Q + I\tan(\phi/2)]/[\cos(\phi/2) - \sin(\phi/2)\tan(\phi/2)]$$

The denominators of both expressions in Equations (17) are identical, so the in-phase and quadrature gains are the same if neither are calculated. The maximum denominator value is 1 when $\phi = 0°$, and the minimum value is 0.997144 when ϕ is 5°, for a maximum signal power effect of 0.025 dB. The denominator value only needs to be calculated if extremely accurate carrier power measurements are needed. Removing the denominators results in the final correction equations:

$$I = A\cos(\Theta) = [I + Q\tan(\phi/2)] \qquad (18)$$
$$Q = A\sin(\Theta) = [Q + I\tan(\phi/2)]$$

A functional block diagram of an embodiment of a phase correction circuit and algorithm 90 of the present invention is shown in FIGURE 5. Circuit and algorithm 90 include summers 92 and 93 receiving the in-phase and quadrature signals, respectively, which already have been corrected for offset and gain errors. Summers 92 and 93 are coupled to the inputs of a multiplier 96, the output is coupled to an integrator 98. Integrator 98 is coupled to a multiplier implemented by a shifter 100, and the output is supplied to a circuit block 102 which divides the shifter output by -1 and multiplies it by the I^2 or Q^2 value from squarer 66 or 67 and passed through a lowpass filter from gain correction circuit 60 shown in FIGURE 3. The output from block 102 is an estimate of $\tan(\phi/2)$, and is provided to both multipliers 104 and 105, which also receives the quadrature or in-phase input signals, respectively. The output of multipliers 104 and 105 are coupled to summers 92 and 93, respectively.

In operation, the in-phase and quadrature inputs are both multiplied by the estimate of $\tan(\phi/2)$ at multipliers 104 and 105, and the result is summed with the other input to form the corrected in-phase and quadrature values. The corrected outputs are multiplied together at multiplier 96 to detect the phase error, and the resulting signal is integrated and shifted. The shifter output is divided by minus 1 times the filtered I^2 or Q^2 output from the gain correction algorithm, resulting in the estimate of $\tan(\phi/2)$.

Since the loop bandwidth is narrow, divider 102 may be operated at a lower sample rate than the signal paths, allowing a low complexity serial divider to be used in implementation.

The phase correction algorithm of the present invention may not function properly when no signal input is present. The presence of an input signal may be detected by a feedback loop enable circuit 97 shown coupled to the output of multiplier 96, for example. The phase correction loop may be disabled until an input signal is detected. Feedback loop enable circuit 97 may also be used to disable the phase correction loop until the gain correction loop has stabilized and produces errors less than a predetermined threshold, for example.

Preferably, phase correction follows gain correction, since the amplitude values are assumed to be equal in derivation.

In implementation, it may be desirable to couple a phase correction value controller 101, such as a symmetric limiter, at the output of shifter 100 to limit the range of phase correction values. Processor controlled calibration may be added to this circuit to

compensate for temperature variation using an approach similar to those described above for offset and gain correction.

The implementation of the phase correction multipliers may take advantage of the limited range of the $\tan(\phi/2)$ value. Assume that the maximum allowable corrected error is $\pm 0.2°$. Correction of a maximum phase range of $\pm 5°$ and setting error of $\pm 0.2°$ requires phase correction multipliers having a maximum gain of $\pm\tan(2.5°)$ and setting error of $\pm\tan(0.1°)$. Given a tangent-linear control signal and multiplier, settings of $-\tan(2.4°$ degrees) to $+\tan$ (2.4° degrees) in 0.2° degree steps (25 total) meet the requirement.

A maximum phase error of +5° corresponds to a maximum linear correction value of $\tan(+2.5°) = +0.043661$, and a minimum phase error of -5° corresponds to a minimum linear correction value of $\tan(-2.5°) = -0.043661$. The maximum input control value corresponds to a right shift of $-\log_2(0.043661) = 4.52$, or over 4 bits. The maximum value of $\tan(\phi/2)$ is then less than 1/16. Assuming four magnitude bits and one sign bit (32 total steps) are adequate for representing the control value, some possible multiplication factors are shown in Table B below

Control Bits	Control Value	Factor= Value/256	$\tan^{-1}$(Factor), deg.	Δ Deg., Prev. $\tan^{-1}$
01100	+12	+0.046875	+2.6838	N/A
01011	+11	+0.042969	+2.4604	0.2234
01010	+10	+0.039063	+2.2370	0.2234
01001	+9	+0.035156	+2.0135	0.2235
--	--	--	--	--
00010	+2	+0.007813	+0.4476	N/A
00001	+1	+0.003906	+0.2238	0.2238
00000	0	0.000000	0.0000	0.2238
11111	-1	-0.003906	-0.2238	0.2238
11110	-2	-0.007813	-0.4476	0.2238
--	--	--	--	--
10111	-9	-0.035156	-2.0135	N/A
10110	-10	-0.039063	-2.2370	0.2235
10101	-11	-0.042969	-2.4604	0.2234
10100	-12	-0.046875	-2.6838	0.2234

TABLE B

The results show that the required range can be met with control settings of +12 to -12, well within the five-bit range of +15 to -16. The worst case phase step due to resolution limits is 0.2238°. The worst case setting error due to resolution limitations is then $\pm$0.2238/2 = $\pm$0.1119°, which is just over the specified limit of $\pm$0.1°.

Phase correction multipliers 104 and 105 may have a five-bit two's complement control value inputs. The outputs of the multipliers are shifted right 8 bits (1/256) from the LSB of the input signal. Further multiplier logic reductions can be realized through truncation and/or rounding prior to the output, since several of the multiplier output LSBs may not be utilized by correction summers 92 and 93.

Simulation of phase correction circuit and algorithm 90 showed that worst case theoretical performance may be achieved with a correction signal from multipliers 104 and 105 having higher resolution than the input signal. A signal-to-noise ratio of at least the minimum theoretical value of 43.9 dB is not achieved until a correction value quantization of 1/4 input LSB is reached.

Simulation also shows that $\tan(\phi/2)$ must be quantized to at least $\mathrm{rnd}(\tan*256)/256$ to achieve a signal-to-noise ratio that is at least the minimum theoretical value of 43.9 dB. The maximum value of $\mathrm{rnd}(\tan(\phi/2)*256)$ is 12 for $\phi = 5°$, indicating that a five-bit two's complement value may be used to represent both positive and negative values of $\tan(\phi/2)$.

It may be advantageous to note that the description set forth above is directed to the functional aspects of the various circuit blocks and the algorithm used to accomplish the error correction. Therefore, the present invention is not limited to any specific implementation of the functional blocks or the algorithms.

Although several embodiments of the present invention and its advantages have been described in detail, it should be understood that mutations, changes, substitutions, transformations, modifications, variations, and alterations can be made therein without departing from the teachings of the present invention, the spirit and scope of the invention being set forth by the appended claims.

WHAT IS CLAIMED IS:

1. Apparatus for quadrature tuner error correction comprising:

an offset correction circuit receiving a digital in-phase signal and a digital quadrature signal from a quadrature tuner, the offset correction circuit having an in-phase circuit comprising:

a summer receiving the digital in-phase signal, subtracting an in-phase offset estimate therefrom, and generating an offset corrected in-phase signal; and

a feedback loop adapted to generating the in-phase offset estimate;

the offset correction circuit having a quadrature circuit comprising:

a summer receiving the digital quadrature signal, subtracting a quadrature offset estimate therefrom, and generating an offset corrected quadrature signal; and

a feedback loop adapted to generate the quadrature offset estimate.

2. The apparatus, as set forth in claim 1, wherein the feedback loop of the in-phase circuit and quadrature circuit each comprises an integrator coupled to the summer receiving the offset corrected in-phase or quadrature signal and operable to integrate the offset corrected in-phase or quadrature signal.

3. The apparatus, as set forth in claim 1, wherein the feedback loop of the in-phase circuit and quadrature circuit each comprises a shifter coupled to the integrator and receiving the integrated offset corrected in-phase or quadrature signal as an input and operable to right shift the input N bits to generate the in-phase or quadrature offset estimate.

4. The apparatus, as set forth in claim 1, wherein the offset correction circuit further comprises an offset correction value controller coupled to the feedback loop receiving a control input, and operable to control levels of the in-phase and quadrature offset estimates.

5. The apparatus, as set forth in claim 1, further comprising a gain correction circuit adapted to receive the offset corrected in-phase signal and the offset corrected quadrature signal, the gain correction circuit comprising:

a first multiplier receiving the offset corrected in-phase signal for multiplication with an inverse of a gain correction estimate, and generating a gain correction in-phase signal;

a second multiplier receiving the offset corrected quadrature signal for multiplication with the gain correction estimate, and generating a gain corrected quadrature signal; and

a feedback loop comprising:

a squaring network coupled to the first and second multipliers and receiving and squaring the gain corrected in-phase and quadrature signals;

a summer coupled to receive signals from the squaring network to subtract the squared quadrature signal from the squared in-phase signal, and generating a difference signal;

an integrator coupled to receive the difference signal from the summer to integrate the difference signal; and

a shifter coupled to the integrator to receive the integrated difference signal, multiply the integrated difference signal by an adjustable constant, and generate the gain correction estimate.

6. The apparatus, as set forth in claim 5, wherein the feedback loop of the gain correction circuit further comprises a feedback loop enable circuit coupled to the squaring network operable to enable the feedback loop upon meeting a certain predetermined condition.

7. The apparatus, as set forth in claim 3, wherein the first and second multipliers of the gain correction circuit each comprises:

a multiplier receiving the offset corrected in-phase or quadrature signal for multiplication by a value within a predetermined range, and generating an output; and

a summer coupled to the multiplier and receiving the output therefrom for summing with the offset corrected in-phase or quadrature signal.

8. The apparatus, as set forth in claim 4, further comprising a phase correction circuit adapted to receive the gain corrected in-phase signal and the gain corrected quadrature signal, the phase correction circuit comprising:

a first multiplier receiving and multiplying the gain corrected quadrature signal with a phase correction factors to generate an in-phase phase correction signal;

a second multiplier receiving and multiplying the gain corrected in-phase signal with the phase correction factor to generate a quadrature phase correction signal;

a first summer coupled to receive the gain corrected in-phase signal and the in-phase phase correction signal from the first multiplier to generate a phase corrected in-phase signal output;

a second summer coupled to receive the gain corrected quadrature signal and the quadrature phase correction signal from the second multiplier to generate a phase corrected quadrature signal output; and

a feedback loop comprising:

a third multiplier coupled to the first and second summers and adapted to multiply the phase corrected in-phase signal output and the phase corrected quadrature signal output to generate a phase error signal;

an integrator coupled to the third multiplier and adapted to integrate the phase error signal;

a shifter coupled to the integrator and adapted to multiply the integrated phase error signal by an adjustable constant to generate a shifted phase error signal; and

a circuit coupled to the shifter and adapted to receive the shifted phase error signal, divide it by -1 and multiply it by the lowpass filtered squared signal from the gain correction circuit, and generate the phase correction factor.

9. The apparatus, as set forth in claim 8, wherein the phase correction factor is $\tan(\phi/2)$, where ϕ is the estimated phase error.

10. The apparatus, as set forth in claim 8, wherein the feedback loop further comprises a feedback loop enable circuit operable to enable the feedback loop of the phase correction circuit in response to the presence of input signals to the first and second summers.

11. The apparatus, as set forth in claim 8, wherein the feedback loop further comprises a feedback loop enable circuit adapted to enable the feedback loop in response to the detection of stable functioning of the gain correction circuit.

12. The apparatus, as set forth in claim 8, wherein the first and second multipliers of the phase correction circuit each comprises:

a multiplier receiving the gain corrected in-phase or quadrature signal, multiplying it by a value within a predetermined range, and generating an output; and

a summer coupled to the multiplier receiving the output therefrom and summing it with the gain corrected in-phase or quadrature signal.

13. A method of correcting tuner quadrature errors, comprising:

an offset correction process receiving a digital in-phase signal and a digital quadrature signal, the offset correction process having an in-phase process comprising:

receiving the digital in-phase signal, subtracting an in-phase offset estimate therefrom, and generating an offset corrected in-phase signal;

integrating the offset corrected in-phase signal;

multiplying the integrated offset corrected in-phase signal by a first adjustable constant; and

generating the in-phase offset estimate;

the offset correction process also having a quadrature process comprising:

receiving the digital quadrature signal, subtracting a quadrature offset estimate therefrom, and generating an offset corrected quadrature signal;

integrating the offset corrected quadrature signal;

multiplying the integrated offset corrected quadrature signal by a second adjustable constant; and

generating the quadrature offset estimate.

14. The method, as set forth in claim 13, wherein generating the in-phase offset estimate, comprises:

integrating the offset corrected in-phase or quadrature signal; and

right shifting the integrated offset corrected in-phase signal N bits and generating the in-phase or quadrature offset estimate.

15. The method, as set forth in claim 13, wherein the in-phase and quadrature process of the offset correction process each comprises high pass filtering the in-phase or quadrature signal with an adjustable cut-off frequency.

16. The method, as set forth in claim 13, further comprising limiting the range of values of the in-phase or quadrature offset estimate.

17. The method, as set forth in claim 13, further comprising a gain correction process receiving the offset corrected in-phase signal and the offset corrected quadrature signal, the gain correction process comprising:

receiving the offset corrected in-phase signal, multiplying it with an inverse of a gain correction estimate, and generating a gain corrected in-phase signal;

receiving the offset corrected quadrature signal, multiplying it with the gain correction estimate, and generating a gain corrected quadrature signal;

squaring the gain corrected in-phase signal;

squaring the gain corrected quadrature signal; subtracting the squared quadrature signal from the squared in-phase signal and generating a difference signal; and

integrating the difference signal; and

multiplying the integrated difference signal by an adjustable constant and generate the gain correction estimate.

18. The method, as set forth in claim 17, further comprising:

detecting the presence of offset corrected in-phase and quadrature signals; and

enabling the gain correction process in response to detecting the signals.

19. The method, as set forth in claim 17, wherein the gain correction process further comprises:

lowpass filtering the offset corrected in-phase signal;

generating an absolute value of the lowpass filtered offset corrected in-phase signal;

comparing the absolute value of the lowpass filtered offset corrected in-phase signal with a predetermined maximum offset value;

lowpass filtering the offset corrected quadrature signal;

generating an absolute value of the lowpass filtered offset corrected quadrature signal;

comparing an abolute value of the lowpass filtered offset corrected quadrature signal with the predetermined maximum offset value; and

enabling the gain correction process in response to the absolute values both being less than the predetermined maximum offset value.

20. The method, as set forth in claim 17, gain corrected in-phase and quadrature comprising limiting the range of the gain correction estimate.

21. The method, as set forth in claim 17, wherein multiplying offset corrected in-phase and quadrature signals by the gain correction estimate each comprises:

multiply the offset corrected in-phase signal or the offset corrected quadrature signal by a value within a predetermined range, and generating an output; and

summing the output with the offset corrected in-phase or quadrature signal.

22. The method, as set forth in claim 18, further comprising a phase correction process receiving the gain corrected in-phase signal and the gain corrected quadrature signal, the phase correction process comprising:

multiplying the gain corrected quadrature signal with a phase correction factor, and generating an in-phase phase correction signal;

multiplying the gain corrected in-phase signal with the phase correction factor and generating a quadrature phase correction signal;

summing the gain corrected in-phase signal and the in-phase phase correction signal and generating a phase corrected in-phase signal output;

summing the gain corrected quadrature signal and the quadrature phase correction signal and generating a phase corrected quadrature signal output;

multiplying the phase corrected in-phase signal output and the phase corrected quadrature signal output, and generating a phase error signal;

integrating the phase error signal;

multiplying the integrated phase error signal by an adjustable constant, and generating a shifted phase error signal; and

dividing the shifted phase error signal by -1 and multiplying by the lowpass filtered and squared signal from the gain correction process, and generating the phase correction factor.

23. The method, as set forth in claim 22, wherein the phase correction process determines:

$$I = I + Q \tan(\phi/2)$$

$$Q = Q + I \tan(\phi/2)$$

where ϕ is the phase correction factor.

24. The method, as set forth in claim 22, wherein the phase correction process further comprises generating an enable signal in response to the presence of input signals to the quadrature tuner, the enable signal being used to enable the phase correction process.

25. The method, as set forth in claim 22, wherein multiplying of the gain corrected quadrature signal with the phase correction factor and the multiplying of the gain corrected in-phase signal with the phase correction factor each comprises:

multiplying gain corrected in-phase or quadrature signal by a value within a predetermined range, and generating an output; and

summing the output with the gain corrected in-phase or quadrature signal.

26. Apparatus for quadrature tuner error correction comprising:

an offset correction circuit adapted to receive a digital in-phase signal and a digital quadrature signal from a quadrature tuner, and generating offset corrected in-phase and quadrature signals;

a gain correction circuit coupled to the offset correction circuit adapted to receive the offset corrected in-phase and quadrature signals and generating offset and gain corrected in-phase and quadrature signals; and

a phase correction process coupled to the gain correction circuit adapted to receive the gain corrected in-phase and quadrature signals and generating offset, gain and phase corrected in-phase and quadrature signals.

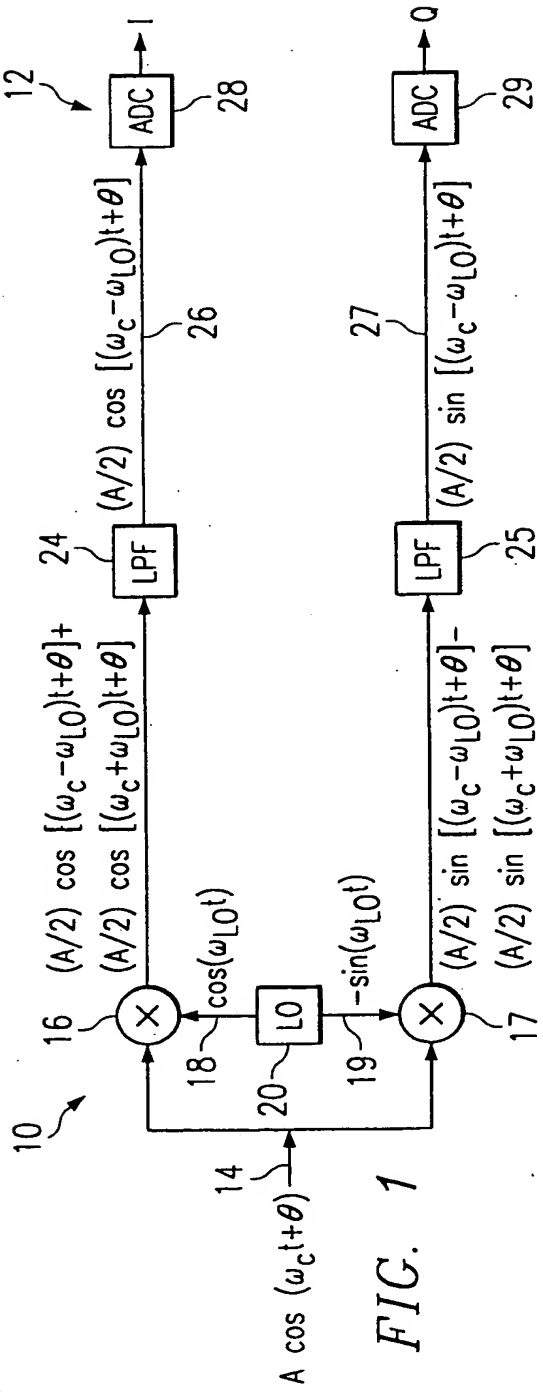
10
12
14
16
17
18
19
20
24
25
26
27
28
29
ADC
ADC
LPF
LPF
LO
I
Q
A cos (ωct+θ)
(A/2) cos [(ωc-ωLO)t+θ]+
(A/2) cos [(ωc+ωLO)t+θ]
(A/2) sin [(ωc-ωLO)t+θ]-
(A/2) sin [(ωc+ωLO)t+θ]
cos(ωLOt)
-sin(ωLOt)
(A/2) cos [(ωc-ωLO)t+θ]
(A/2) sin [(ωc-ωLO)t+θ]

FIG. 1

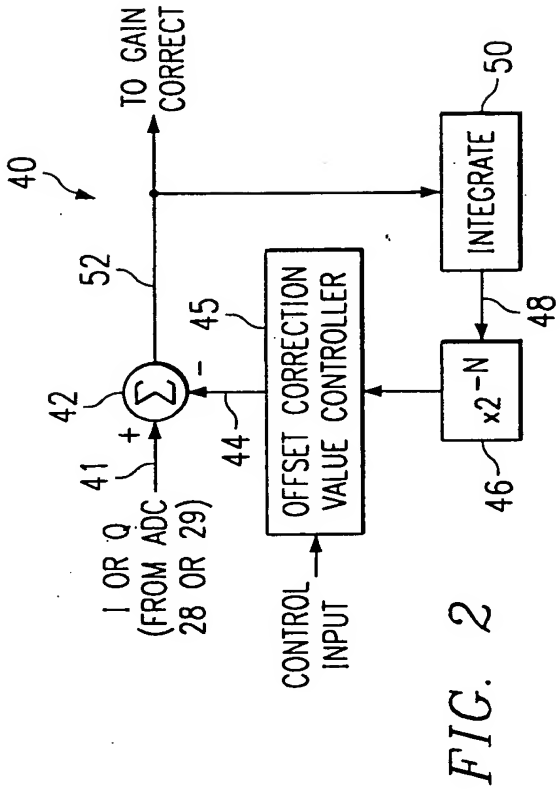
40
41
42
44
45
46
48
50
52
TO GAIN CORRECT
I OR Q (FROM ADC 28 OR 29)
CONTROL INPUT
OFFSET CORRECTION VALUE CONTROLLER
INTEGRATE
x2-N
+
-

FIG. 2

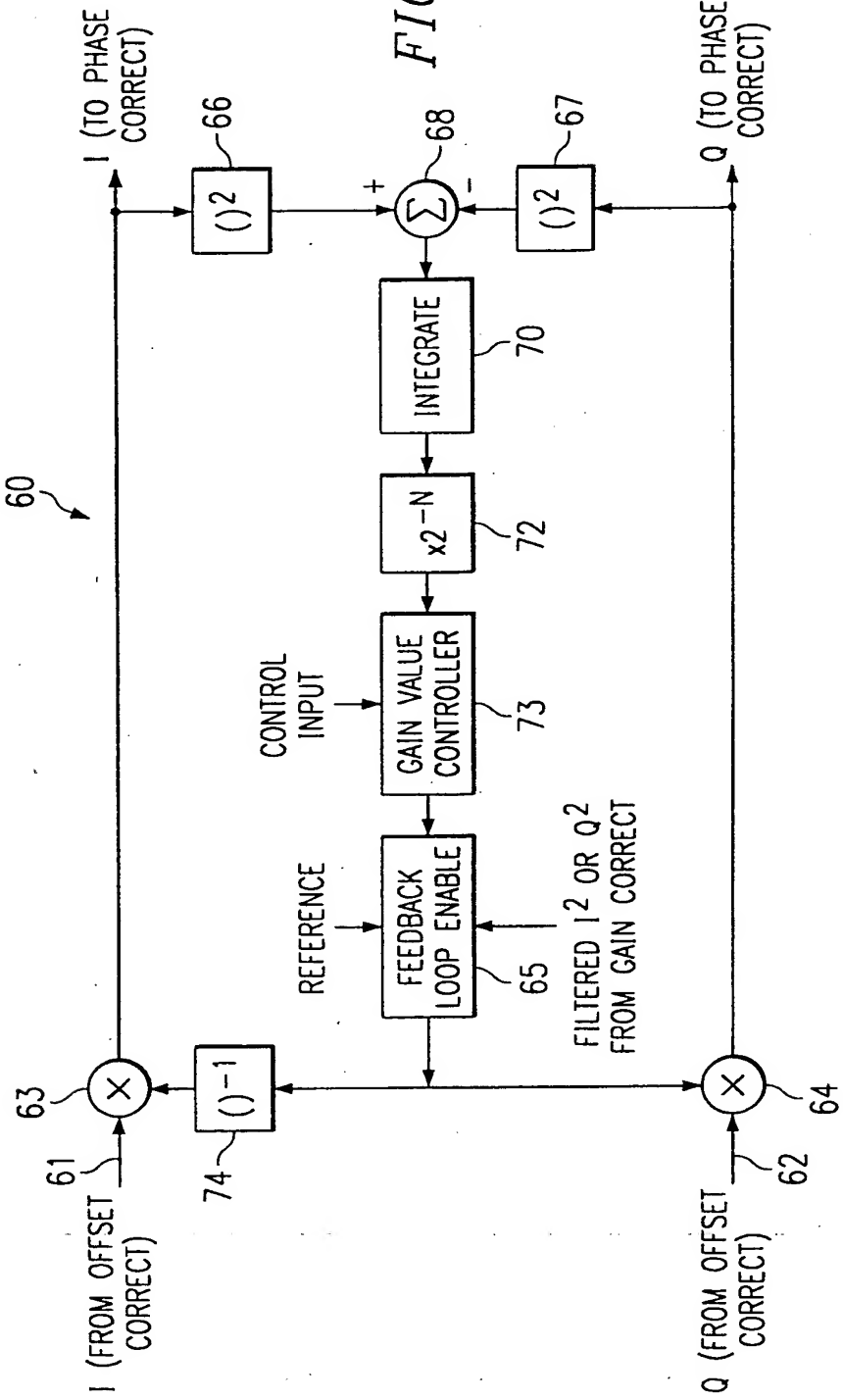
I (TO PHASE CORRECT)
Q (TO PHASE CORRECT)
66
67
68
INTEGRATE
70
x2^-N
72
GAIN VALUE CONTROLLER
73
CONTROL INPUT
FEEDBACK LOOP ENABLE
65
REFERENCE
FILTERED I^2 OR Q^2 FROM GAIN CORRECT
60
63
64
61
62
74
I (FROM OFFSET CORRECT)
Q (FROM OFFSET CORRECT)

FIG. 3

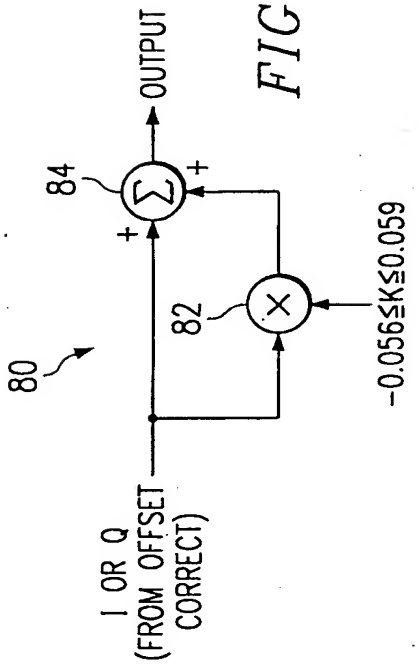
80
84
82
OUTPUT
I OR Q (FROM OFFSET CORRECT)
-0.056≤K≤0.059

FIG. 4

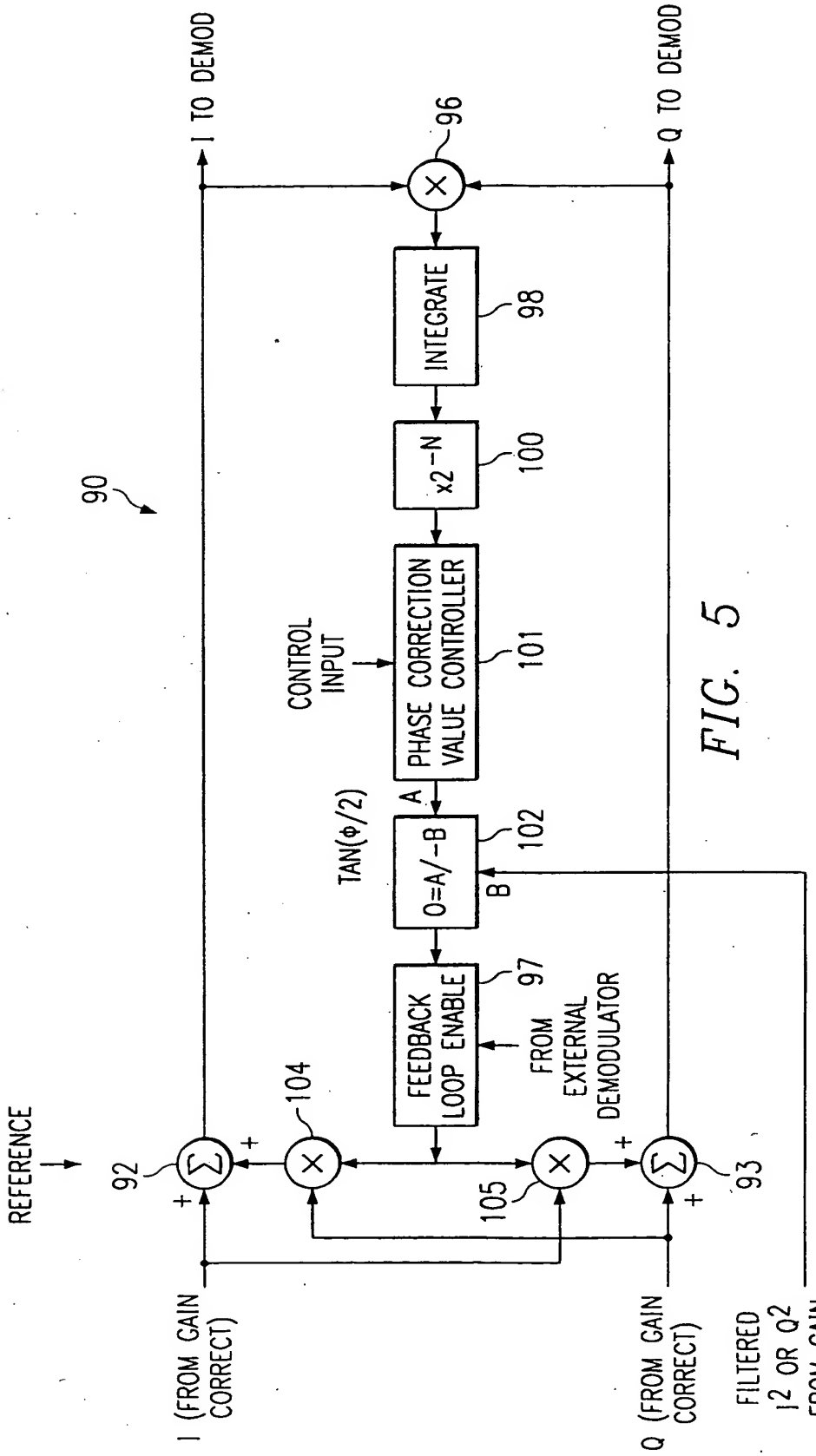
I TO DEMOD
Q TO DEMOD
96
INTEGRATE
98
x2^-N
100
90
CONTROL INPUT
PHASE CORRECTION VALUE CONTROLLER
101
TAN(Φ/2)
A
O=A/-B
102
B
FEEDBACK LOOP ENABLE
97
FROM EXTERNAL DEMODULATOR
REFERENCE
92
104
105
93
I (FROM GAIN CORRECT)
Q (FROM GAIN CORRECT)
FILTERED I² OR Q² FROM GAIN CORRECT

FIG. 5

INTERNATIONAL SEARCH REPORT

Interna al Application No
PCT/US 00/20060

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03D3/00 H04L25/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03D H04L H03C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
PAJ, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 196 16 368 C (HAGENUK MARINEKOMMUNIKATION GM) 11 December 1997 (1997-12-11)	1,13,26
A	page 4, line 14 -page 7, line 30; figure 2	5,17,18, 22
A	EP 0 392 229 A (ANT NACHRICHTENTECH) 17 October 1990 (1990-10-17) column 3, line 28 - line 65; figure 1	1-3,13, 14,17

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 November 2000	10/11/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Ratajski, A

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Internal Application No
PCT/US 00/20060

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	ASCHWANDEN F: "DIRECT CONVERSION - HOW TO MAKE IT WORK IN TV TUNERS" IEEE TRANSACTIONS ON CONSUMER ELECTRONICS,US,IEEE INC. NEW YORK, vol. 42, no. 3, 1 August 1996 (1996-08-01), pages 729-738, XP000638561 ISSN: 0098-3063 page 730, column 1, line 18 -page 732, column 2, line 14; figure 2	1,13,26

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 00/20060

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 19616368 C	11-12-1997	NONE	
EP 0392229 A	17-10-1990	DE 3911486 A	11-10-1990
		AT 122192 T	15-05-1995
		DE 59008997 D	08-06-1995